**E.G.S. PILLAY ENGINEERING COLLEGE**

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| ALL COS |
| Regulations 2023 |
| **AIDS** |

(*Autonomous*) Nagapattinam – 611 002

Second Year / Third semester

**2301GEX05 – APPLIED DIGITAL LOGIC AND DESIGN**

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| **PART A (Marks :10 \*2 = 20)** | | **Marks** | **CO** | **BTL** |
| **Course Outcome : 01** | | | | |
| 1 | Name the two basic types of Boolean expressions. | 2 | CO1 | L2 |
| 2 | *Simplify the Boolean function F=AB+ BC + B*′*C.* | 2 | CO1 | L2 |
| 3 | Convert decimal number 650 into its hexadecimal equivalent. | 2 | CO1 | L2 |
| 4 | Simplify A+AB+A’+B. | 2 | CO1 | L2 |
| 5 | Describe number system and write its types. | 2 | CO1 | L2 |
| 6 | Convert (725.63)8 to binary. | 2 | CO1 | L2 |
| 7 | Specify the methods adopted to reduce Boolean function. | 2 | CO1 | L2 |
| 8 | Describe the prime implicants. | 2 | CO1 | L2 |
| 9 | List out the advantages of K – map method. | 2 | CO1 | L2 |
| 10 | Express in algorithm for generating prime implicants. | 2 | CO1 | L2 |
| **Course Outcome : 02** | | | | |
| 1 | Enumerate some of the combinational circuits. | 2 | CO2 | L2 |
| 2 | Discuss BCD adder. | 2 | CO2 | L2 |
| 3 | What is code conversion? | 2 | CO2 | L2 |
| 4 | Implement the following function using suitable multiplexer.  F(x , y ,z) = ∑m (0 ,2 ,5 ,7). | 2 | CO2 | L2 |
| 5 | Design a single bit magnitude comparator two words A and B. | 2 | CO2 | L2 |
| 6 | Design a three bit even parity generator. | 2 | CO2 | L2 |
| 7 | Write the procedure to design code converters. | 2 | CO2 | L2 |
| 8 | What is a data selector? | 2 | CO2 | L2 |
| 9 | List out the application of multiplexer. | 2 | CO2 | L2 |
| 10 | Suggest a solution to overcome the limitation on the speed of an adder. | 2 | CO2 | L2 |

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| **PART A (Marks :10 \*2 = 20)** | | **Marks** | **CO** | **BTL** |
| **Course Outcome : 03** | | | | |
| 1 | Demonstrate latch. | 2 | CO3 | L2 |
| 2 | Classify different types of flip flops. | 2 | CO3 | L2 |
| 3 | Relate With reference to a JK flip flop, what is racing. | 2 | CO3 | L2 |
| 4 | Give the characteristic equation and state diagram of JK flip flop. | 2 | CO3 | L2 |
| 5 | How many flip flops are needed to build an 8 bit shift register? | 2 | CO3 | L2 |
| 6 | Write applications of shift registers. | 2 | CO3 | L2 |
| 7 | Draw the state diagram of MOD – 10 counter. | 2 | CO3 | L2 |
| 8 | Illustrate the different types of counter. | 2 | CO3 | L2 |
| 9 | Form the truth table for 3 – bit binary down counter. | 2 | CO3 | L2 |
| 10 | Classify hazards and its types. | 2 | CO3 | L2 |
| **Course Outcome : 04** | | | | |
| 1 | Give the features of a ROM cell. | 2 | CO4 | L2 |
| 2 | Write classification of RAM and describe it. | 2 | CO4 | L2 |
| 3 | Compare between volatile and non – volatile memory. | 2 | CO4 | L2 |
| 4 | Summarize the access time and cycle time of a memory. | 2 | CO4 | L2 |
| 5 | Outline the ‘write operation’ with an example. | 2 | CO4 | L2 |
| 6 | Whether PAL is same as PLA? Explain. | 2 | CO4 | L2 |
| 7 | Demonstrate PLD. | 2 | CO4 | L2 |
| 8 | Mention few applications of PLA and PAL. | 2 | CO4 | L2 |
| 9 | classify the PLDs. | 2 | CO4 | L2 |
| 10 | Why the input variables to a PAL are buffered? | 2 | CO4 | L2 |

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| **PART A (Marks :10 \*2 = 20)** | | **Marks** | **CO** | **BTL** |
| **Course Outcome : 05** | | | | |
| 1 | Write a short notes for the need of HDL. | 2 | CO5 | L2 |
| 2 | Contrast the structure of a Verilog module. | 2 | CO5 | L2 |
| 3 | Verilog supports which three modeling techniques. | 2 | CO5 | L2 |
| 4 | Design a 3 input AND gate using Verilog. | 2 | CO5 | L2 |
| 5 | Are Verilog and VHDL the same , describe it. | 2 | CO5 | L2 |
| 6 | Which kinds of operators Verilog supports? | 2 | CO5 | L2 |
| 7 | Summarize Verilog data types. | 2 | CO5 | L2 |
| 8 | Write a program for below circuit  And Gate Picture | 2 | CO5 | L2 |
| 9 | Verilog HDL code in behavioral model of a D – latch. | 2 | CO5 | L2 |
| 10 | What is Verilog used for? | 2 | CO5 | L2 |

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| **PART B (16 Marks)** | | **Marks** | **CO** | **BTL** |
| **Course Outcome : 01** | | | | |
| 1 | a) *Simplify the Boolean function i)F = A + A’B ii) F = AB+BC+B’C .*  b) Plot Boolean expression Y = ABC’ + ABC + A’B’C on the Karnaugh map. | 8  8 | CO1 | L3 |
| 2 | a) Simplify the following expression using K -map method.  Y = ∑ m (7 , 9 , 10 , 11 ,12 ,13, 14, 15).  b) Plot Boolean expression Y = (A+B’+C) (A+B’+C’) (A’+B’+C) (A+B+C’) on  the Karnaugh map. | 8  8 | CO1 | L3 |
| 3 | a) Solve the reduced SOP form of the following function  f(A,B,C,D) = ∑ m (1, 3, 7, 11, 15) + ∑d (0 , 2, 4).  b) State and prove De Morgan’s theorem with logic diagram. | 8  8 | CO1 | L3 |
| 4 | a) Reduce the following function using K – map technique.  F(A,B,C,D) = ∑m (5 , 6, 7, 12, 13) + ∑d (4 , 9, 14, 15).  b) *Simplify the Boolean function F = AB + (AC)′ + AB′C(AB + C).* | 8  8 | CO1 | L3 |
| 5 | Solve the following Boolean function by using a tabulation method.  F(A,B,C,D) = ∑ m (0, 2, 3, 6, 7, 8, 10, 12, 13). | 16 | CO1 | L3 |
| 6 | Minimize the expression using tabulation method.  Y = A’BC’D’ + A’BC’D + ABC’D’ + ABC’D + AB’C’D + A’B’CD’ . | 16 | CO1 | L3 |
| **Course Outcome : 02** | | | | |  |  |  | K2 |
| 1 | 1. Design a combination logic circuit with three input variables that will produce a logic 1 output when more than one input variables are logic 1. 2. Design the logic circuit for full adder. | 8  8 | CO2 | L3 |
| 2 | 1. Design a full subtractor. 2. Design a combinational circuit with three inputs and one output.   i)The output is 1 When the binary value of the input is less than 6. Otherwise output is 0 . | 8  8 | CO2 | L3 |
| **3** | 1. Implement an even and odd parity generator for 3 – bit input data , check for parity Error. 2. Write design procedure of the combinational circuit. | 12  4 | CO2 | L3 |
| 4 | 1. Design 2 – bit magnitude comparator using gates. 2. Write comparison between combinational circuits.   1.Decoder Vs Demultiplexer.  2.Encoder Vs Multiplexer. | 12  4 | CO2 | L3 |
| 5 | 1. What is multiplexer? Design 4 :1 multiplexer and draw the logic diagram. 2. What is decoder? Design 2 to 4 binary decoder and draw the logic circuit. | 8  8 | CO2 | L3 |
| 6 | 1. Design a logic circuit for 4 bit binary to BCD convertor. 2. Design 1 : 8 demultiplexer circuit. | 8  8 | CO2 | L3 |
|  | | **Marks** | **CO** | **BTL** |
| **Course Outcome : 03** | | | | |
| 1 | Draw RS flip flop circuit and explain its operations with truth table and suggest how to eliminate the undetermined stage? Write some RS flip flop applications. | 16 | CO3 | L3 |
| 2 | Design a 4 bit binary counter and explain its counting process. Discuss how to use this circuit to perform both up and down counting. | 16 | CO3 | L3 |
| 3 | Design BCD ripple counter using JK flip – flop. | 16 | CO3 | L3 |
| 4 | Describe how a JK flip – flop function and explain its behaviour with different input combination. | 16 | CO3 | L3 |
| 5 | Explain the principle of operation of 4 – bit universal shift register. | 16 | CO3 | L3 |
| 6 | Elaborate on the shift register typesmentioned below?  i)SISO ii)SIPO iii)PISO iv)PIPO | 16 | CO3 | L3 |
| **Course Outcome : 04** | | | | |  |  |  | K2 |
| 1 | Write a descriptive note on memories mentioned below.  i) RAM ii) ROM iii)PROM iv) EPROM v) EEPROM. | 16 | CO4 | L3 |
| 2 | 1. Design 16 K \* 8 RAM using four 4 K \* 8 ICs. 2. A combinational circuit is defined by the function.   F1 = ∑m(3 , 5 , 7) , F2 = ∑m(4 , 5 , 7)  Implement the circuit with a PLA having 3 inputs , 3 product terms and two outputs. | 8  8 | CO4 | L3 |
| **3** | Design using PAL the following Boolean function.  W(A,B,C,D) = ∑(2,12,13)  X(A,B,C,D) = ∑(7,8,9,10,11,12,13,14,15)  Y(A,B,C,D) = ∑(0,2,3,4,5,6,7,8,10,11,15)  Z(A,B,C,D) = ∑(1,2,8,12,13). | 16 | CO4 | L3 |
| 4 | a)Draw a PLA circuit to implement the logic functions  A’BC +AB’C + AC’ and A’B’C’ + BC.  b)Describe the concept , working and application of FPGA. | 8  8 | CO4 | L3 |
| 5 | a)Illustrate the concept of 16 \* 8 bit ROM arrange with diagram.  b)Design 1 K \* 8 RAM using two 1 K \* 4 ICs. | 8  8 | CO4 | L3 |
| 6 | a)Explain DRAM organization .  b)Design and implement 3 bit binary to gray code converter using PLA. | 8  8 | CO4 | L3 |
|  | | **Marks** | **CO** | **BTL** |
| **Course Outcome : 05** | | | | |
| 1 | 1. Write a program for below circuit using Verilog HDL code in behavioral model.   Model Combinational Logic in Verilog   1. Write Verilog HDL code for full adder in data flow description. | 8  8 | CO5 | L3 |
| 2 | 1. Write Verilog HDL code for 4 – bit synchronous counter with parallel load. 2. Write Verilog HDL code in structural model of a ripple counter. | 8  8 | CO5 | L3 |
| 3 | 1. Explain the structure of Verilog HDL program with the help of example. 2. Write application of Verilog HDL. | 8  8 | CO5 | L3 |
| 4 | 1. Develop a Verilog HDL code in structural description of a 2 \* 1 multiplexer with active low enable. 2. Develop a Verilog HDL code for given combinational circuit. | 8  8 | CO5 | L3 |
| 5 | 1. Design a Program in verilog HDL code in structural description for implementation of a full – adder with two half – adders and an OR gate.   Half Adder and Full Adder Circuit with ...   1. Explain boolean logical operators and Relational operators in verilog HDL. | 8  8 | CO5 | L3 |
| 6 | A positive edge triggered flip -flop has two inputs D1 and D2 and a control input that chooses between the two. Write an program in HDL behavioral description of this flip – flop and draw diagram. | 16 | CO5 | L3 |